California State University San Marcos • NEW COURSE • FORM C CS 445

ORIGINATOR'S SECTION:

1. College:

☐ CHABSS ☐ CoBA
☐ CoEHHS ☒ CSM

Desired Term and Year of Implementation (e.g., Fall 2008):

Spring 2018

2.Course is to be considered for G.E.? (If yes, also fill out appropriate GE form*) ☐ Yes ☒ No

3. Course will be a variable-topics (generic) course? ☐ Yes ☒ No
("generic" is a placeholder for topics)

4. Course abbreviation and Number:* CS 445

5. Title: ***(Titles using jargon, slang, copyrighted names, trade names, or any non-essential punctuation may not be used.)***
Reconfigurable Embedded Systems

6. Abbreviated Title for PeopleSoft:
(no more than 25 characters, including spaces)
Reconfig. Embedded Sys.

7. Number of Units: 3

8. Catalog Description: ***(Not to exceed 80 words; language should conform to catalog copy. Please consult the catalog for models of style and format; include all necessary information regarding consent for enrollment, pre- and/or corequisites, repeated enrollment, crosslisting, as detailed below. Such information does not count toward the 80-word limit.)***

Covers concepts, technologies, and programming languages used in modern digital embedded systems. Subjects include general-purpose computing, reconfigurable computing, and application-specific computing in digital system design. Covers technologies of reconfigurable computing systems such as FPGAs (Field Programmable Gate Arrays), design flow and implementation in reconfigurable systems, Hardware Description Languages (HDLs), such as VHDL (Very high speed integrated circuits Hardware Description Language programming, techniques to reconfigure systems over time including partitioning and placement, and on-chip communication solutions in dynamically reconfigurable systems. *May not be repeated for credit by students who have received credit for CS 497-5. Prerequisite: CS 331.*

9. Why is this course being proposed?

This course helps students to understand hardware oriented design and programming (e.g. VHDL) on reconfigurable hardware (e.g. FPGA), while in CS 435, software oriented approaches (e.g. Embedded C) and embedded microprocessors are covered. The students will be exposed to the possibilities and rapidly growing interest in adaptive hardware and corresponding design techniques by providing them with the necessary knowledge for understanding and designing reconfigurable hardware systems and studying applications benefiting from dynamic hardware reconfiguration.

10. Mode of Instruction*

For definitions of the Course Classification Numbers:
http://www.csusm.edu/academic_programs/curriculumscheduling/catalogcurricula/DOCUMENTS/Curricular_Forms_Tab/Instructional%20Mode%20Conventions.pdf

Type of Instruction	Number of Credit Units	Instructional Mode (Course Classification Number)
Lecture	3	C2
Activity		
Lab		

11. Grading Method:*
☒ Normal (N) *(Allows Letter Grade +/-, and Credit/No Credit)*
☐ Normal Plus Report-in-Progress (NP) *(Allows Letter Grade +/-, Credit/No Credit, and Report-in-Progress)*
☐ Credit/No Credit Only (C)
☐ Credit/No Credit or Report-in-Progress Only (CP)

12. If the (NP) or (CP) grading system was selected, please explain the need for this grade option.

13. Course Requires Consent for Enrollment? ☐ Yes ☒ No

☐ Faculty ☐ Credential Analyst ☐ Dean ☐ Program/Department - Director/Chair

14. Course Can be Taken for Credit More than Once? ☐ Yes ☒ No
If yes, how many times? (including first offering)

RECEIVED
MAY 17 2017
BY:

* If Originator is uncertain of this entry, please consult with Program/Department Director/Chair.

15. Is Course Crosslisted: ☐ Yes ☒ No

If yes, indicate which course and check "yes" in item #22 below.

16. Prerequisite(s): ☒ Yes ☐ No CS 331

17. Corequisite(s): ☐ Yes ☒ No

18. Documentation attached:
☒ Syllabus ☐ Detailed Course Outline

19. If this course has been offered as a topic, please enter topic abbreviation, number, and suffix:* Digital Embedded Systems, CS 497-5

20. How often will this course be offered once established?* Once a year

PROGRAM DIRECTOR/CHAIR - COLLEGE CURRICULUM COMMITTEE SECTION:
(Mandatory information – all items in this section must be completed.)

21. Does this course fulfill a requirement for any major (i.e., core course or elective for a major, majors in other departments, minors in other departments)? ☒ Yes ☐ No

If yes, please specify:
Computer Science as an elective course

22. Does this course impact other discipline(s)? (*If there is any uncertainty as to whether a particular discipline is affected, check "yes" and obtain signature.*) ☐ Yes ☒ No

If yes, obtain signature(s). Any objections should be stated in writing and attached to this form.

Discipline _____ _____ _____Support _____Oppose
Signature Date

Discipline _____ _____ _____Support _____Oppose
Signature Date

SIGNATURES : (COLLEGE LEVEL) :

1. Originator (please print or type name) Date
2. Program Director/Chair 4/21/17 Date
3. College Curriculum Committee 5/10/17 Date
4. College Dean (or Designee) 5/10/17 Date

(UNIVERSITY LEVEL)

5. UCC Committee Chair Date
6. Vice President for Academic Affairs (or Designee) Date
7. President (or Designee) Date

Trnkcv

PS

Office of Academic Programs ~~Banner~~ Catalog Revised 3/28/2007

* If Originator is uncertain of this entry, please consult with Program/Department Director/Chair

RP

COURSE SYLLABUS CS 497-5
Reconfigurable Embedded Systems
Spring 2017

Class hours: 10:30-11:45am, Tu Th
Classroom: Markstein Hall 305
Instructor: Dr. Ali Ahmadinia

Course Description

This course covers concepts, technologies, and programming languages used in modern reconfigurable embedded systems. Topics include general-purpose computing, reconfigurable computing, and application-specific computing in digital system design, technologies of reconfigurable computing systems such as FPGAs (Field Programmable Gate Arrays), design flow and implementation in reconfigurable systems, Hardware Description Languages (HDLs) especially VHDL programming, techniques to reconfigure systems over time including partitioning and placement, and on-chip communication solutions in dynamically reconfigurable systems. Applications benefiting from dynamic hardware reconfiguration will be discussed.

Course Prerequisites

CS 331

Learning Outcomes

- Knowledge and understanding of:
  - the types of reconfigurable technologies available today
  - pros and cons of reconfigurable hardware technology
  - Essential design steps and optimization algorithms for FPGAs
  - How and which applications benefiting from FPGAs
- Intellectual
  - Understand leading edge research problems on exploitation of run-time reconfigurable design methodologies including future trends
- Practical
  - Ability to use commercial tools to develop FPGA systems
  - Ability to build a reconfigurable embedded system and program to satisfy given user specifications

Reading Materials and Textbooks

There will be reading assignments, typically papers published by the IEEE and ACM.

Christophe Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications," Springer, 2007.

S. Hauck and A. DeHon, "Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation," Ed., Elsevier, 2008.

Pao-Ann Hsiung, Marco D. Santambrogio, and Chun-Hsian Huang, "Reconfigurable System Design and Verification", CRC Press, 2009

http://www.xilinx.com

http://www.altera.com

Office Hours

The following is the office hours of the instructor. Reasonable appointments will also be accommodated to the best of the instructors' availability. In addition, the instructors will try to be available during the office hours.

Instructor	Office Location	Office Hours	Email
Dr. Ali Ahmadinia	Science II 315	12:00 –13:30pm, Thu or by appointment	aahmadinia@csusm.edu

Disabled Student Services

Students with disabilities who require reasonable accommodations must be approved for services by providing appropriate and recent documentation to the Office of Disabled Student Services (DSS). This office is located in Craven Hall 5205, and can be contacted by phone at (760) 750-4905, or TTY (760) 750-4909. Students authorized by DSS to receive reasonable accommodations should meet with me during my office hours in order to ensure confidentiality.

Academic Honesty

"Students will be expected to adhere to standards of academic honesty and integrity, as outlined in the Student Academic Honesty Policy. All written work and oral presentation assignments must be original work. All ideas/material that are borrowed from other sources must have appropriate references to the original sources. Any quoted material should give credit to the source and be punctuated with quotation marks.

Students are responsible for honest completion of their work including examinations. There will be no tolerance for infractions. If you believe there has been an infraction by someone in the class, please bring it to the instructor's attention. The instructor reserves the right to discipline any student for academic dishonesty, in accordance with the general rules and regulations of the university. Disciplinary action may include the lowering of grades and/or the assignment of a failing grade for an exam, assignment, or the class as a whole."

Incidents of Academic Dishonesty will be reported to the Dean of Students. Sanctions at the University level may include suspension or expulsion from the University.

Course Policies

1. Students should individually work on all homework assignments and turn them in on the class website at the beginning of the class when they are due. No late assignments are accepted unless there is a family or work emergency, in which case you must provide the instructor a valid written proof before the assignment due date. If the reason seems valid, you will be granted an extension.

2. The University writing requirements will be satisfied by written homework assignments as well as course project report.

3. Students are expected to be active learners. Students should read materials posted in Cougar Course before coming to lectures, and are expected to attend all classes and participate in class discussions.

4. The use of computers and mobile devices during the lecture for course unrelated purposes is not permitted. If violated, you may be logged out the computer or asked to leave the classroom.

Grades

Homework Assignments: 30%
Midterm Exam: 15%
Course Project: 20%
Final Exam: 20%
Class Participations and reading assignments: 15%

Your letter grade will be based on the following scale:

Total	≥ 93	$90 \leq$ and < 93	$87 \leq$ and < 90	$83 \leq$ and < 83	$80 \leq$ and < 83	$75 \leq$ and < 80	$70 \leq$ and < 75	< 70
Grade	A	A-	B+	B	B-	C+	C	D

Homework Assignments

Each student will write, debug, and demonstrate a number of VHDL programs for a Xilinx Basys-3 FPGA board using the Xilinx Vivado integrated development environment. These assignments provide hands-on experience and help to build student's embedded hardware programming skills.

Course Project

Students will undertake a project (on a related topic subject to instructor approval) exploring fundamental issues in reconfigurable computer architectures, systems, and applications or design and implement a practical application on an FPGA board. This project will provide students the opportunity to more deeply explore fundamental issues in reconfigurable computing systems. The outcome of each project will be a clear and concise technical report discussing project concepts, development, experiments, results, analyses as well as a demonstration.

Class Participation and Exercises

Students are expected to be active learners. Students should read materials to-be-covered before coming to lectures, and are expected to attend all classes and participate in class discussions and activities. There are regular class exercises to help you to understand the material better and deeper and consolidate your confidence for the exams.

Reading Assignments and Presentations

There will be regular research paper reading assignments. All students need to review the paper and submit a 300 word opinion statement about the paper before the paper is presented in the class.

Tentative Schedule

Week	Topic
1	Introduction to Reconfigurable Systems
2	FPGAs (Field Programmable Gate Arrays)
3-5	VHDL Programming
6-8	A Design and Implementation Cycle Overview
8	Midterm Exam
9	High-Level Synthesis
10-12	Temporal Partitioning and Placement
13-14	On-chip Communication Architectures
15	Course Project Demonstrations
	Final Exam

Please note that this schedule is tentative, and subject to change as deemed appropriate.